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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,896	01/30/2004	Makoto Terui	030712-23	5698

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,896	TERUI, MAKOTO	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-12,14 and 17-22* is/are pending in the application.

4a) Of the above claim(s) *17-19* is/are withdrawn from consideration.

5)☒ Claim(s) *22* is/are allowed.

6)☒ Claim(s) *4-12,14,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claim 20 is rejected under 35 U.S.C. 102(a) as being anticipated by Kishimoto et al. (US Pat. 6603210).

Regarding claim 20, Kishimoto et al. disclose a multichip module (MCM- see Fig. 1 and 5a-5c) comprising a semiconductor chip and a plurality of passive elements/chips (see 6 in Fig. 5a-5c)

- a substrate (1/2/3 in Fig. 1)
- an insulating resin layer (9 in Fig. 1) formed on the substrate
- an inductor (see 6 in Fig. 1 and 5a-5c; Col. 5, line 45) formed/positioned in the insulating layer by a first metal terminal/wire terminal (not numerically referenced in Fig. 1; see edge metal connections of the circuit element 6 in Fig. 5a-5c; col. 10, line 7)
- a capacitor (see 6 in Fig. 1 and 5a-5c; Col. 5, line 45) formed/positioned in the insulating layer by a second metal terminal/wire (not numerically referenced in Fig. 1; see edge metal connections of other circuit element 6 in Fig. 5a-5c; Col. 10, line 7), wherein the capacitor is isolated from the inductor (see Fig. 5a)

- a protective film (4 in Fig. 1) formed on the insulating layer, wherein the protective film has first and second openings for exposing the inductor and capacitor respectively (see openings in 4 having conductive joint 8 in Fig. 1)
- first and second wiring patterns respectively (see 3a in Fig. 1) formed within the first and second openings; and
- the first and second wiring patterns formed for connecting to an external source and other external source respectively (see 12 in Fig. 1 and 5b)

(Fig. 1 and 5a-5c; Col. 4, line 60- Col. 7, line 45; Col. 8, line 50- Col. 10, line 55).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-12, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishimoto et al. (US Pat. 6603210). in view of Maeda et al. (US Pat. 6582991), Lin et al. (US Pat. 2002/0122244) and Panella et al. (US Pat. 6853559).

Regarding claims 4-12, 14 and 21, Kishimoto et al. teach the entire structure as applied to claim 20 above, except the passive elements being of different specifications or being formed on the substrate by metal wires.

Maeda et al. teach a multichip module (MCM) having IC chip elements/components wherein the chip components include a variety of active and passive components (300 and 200 respectively in Fig. 2) wherein the passive component types include conventional resistor, capacitor, etc. each component having respective specifications (resistance, capacitance, inductance, quality factor, etc.), values and dimensions to provide the desired application requirements (Col. 13, lines 20-35). Furthermore, the elements/components include those of the same or different types (see Fig. 18, 19, etc.) as per application requirements (Col. 28, line 33- Col 30, line 15)

Lin et al. teach a MCM having a variety of conventional passive devices/chip components (644 in Fig. 11A) including capacitor, inductor, etc. wherein the inductor and the capacitor are formed on a substrate by spirally disposed metal pattern/wires and conventional capacitor configuration including parallel wiring layers/electrode layers respectively (see 642a in Fig. 11A and Fig. 10B respectively; section 0072). Lin et al. further teach the chip components/passive devices being formed/diced from a wafer using a conventional wafer scale processing (sections 0006-00010).

Kishimoto et al. further teach the terminals of the passive elements/chips being connected by second/external electrodes covered by an insulating/protective resin layer (see 12 and 11 respectively in Fig. 1).

Panella et al. teach an IC system integration comprising active/passive IC chips/components including resistor, capacitor, etc. wherein the chips/components include those having high/low frequency specifications, the system configuration further include the components being configured/divided into groups including high and low frequency specifications to provide the desired power/signal and performance requirements and improved electromagnetic interference (EMI) protection and thermal management (see col. 2, 5, 9, 22-28; Fig. 1-19).

Furthermore, the determination of parameters such as number of passive components, types, grouping according to the specifications including frequency characteristics and other performance parameters in a multichip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired application requirements, module performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of passive elements having different specifications, being formed on the substrate by metal wires and being divided into a plurality of groups having mutually different specifications or groups including high and low frequency specifications as taught by Maeda et al., Lin et al. and Panella et al. so

that the desired device integration, performance and reliability can be achieved in Kishimoto et al's MCM.

Allowable Subject Matter

5. Claim 22 is allowed.

Reasons for Allowance

6. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "a passive element chip within the insulating film and being formed on the first substrate, and a semiconductor chip within the insulating film and being formed on the first substrate" and "wherein the passive element chip comprises a second substrate different from the first substrate; an insulating layer formed on the second substrate; an inductor formed in the insulating layer by a first metal wire; a capacitor formed in the insulating layer by a second metal wire, with the capacitor being isolated from the inductor" in a highly integrated module having active and passive components within an insulating film on a substrate.

Response to Arguments

7. Applicant's arguments with respect to claims 4-12, 14, 20 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

11-26-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800